AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A package containing a semiconductor element comprising:

a housing containing a semiconductor element, ~~said housing having two primary side walls that are perpendicular to each other~~; and

a pair of positioning holes and a pair of attaching holes respectively provided at opposed side portions of said housing;

wherein a line between said pair of positioning holes and a line between said pair of attaching holes intersect with each other substantially at a center of said package and further wherein the line between the positioning holes is skewed with respect to each of ~~the two~~ four primary side walls of the housing and the line between the attaching holes is skewed with respect to each of the four primary side walls such that the line between the positioning holes and the line between the attaching holes are each neither parallel nor perpendicular to ~~either~~ any of the primary side walls, and further wherein neither line is located at a center line of the device, such that it is perpendicular to any of the primary side walls.

2. (Original) The package according to claim 1:

wherein said semiconductor element is a solid-state imaging element.

3. (Currently Amended) A semiconductor device comprising:

a semiconductor element;

a housing containing said semiconductor element, ~~said housing having two primary side walls that are perpendicular to each other~~; and

a pair of positioning holes and a pair of attaching holes respectively provided at opposed side portions of said housing;

wherein a line between said pair of positioning holes and a line between said pair of attaching holes intersect with each other substantially at a center of said package and further wherein the line between the positioning holes is skewed with respect to each of ~~the two~~ four primary side walls of the housing and the line between the attaching holes is skewed with respect to each of the four primary side walls such that the line between the positioning holes and the line between the attaching holes are each neither parallel nor perpendicular to ~~either~~ any of the primary side walls, and neither line is located at a center line of the decice which is perpendicular to the primary side walls.

4. (Original) The semiconductor device according to claim 3,

wherein said semiconductor element is a solid-state imaging element.

5. (Currently Amended) A semiconductor device comprising:

a semiconductor element;

a housing containing said semiconductor element, ~~said housing having two primary side walls that are perpendicular to each other~~;

a pair of attaching holes provided at opposed side portions of said housing at a surface of said package; and

a transparent member for sealing said semiconductor element in a recess portion;

wherein said surface of said housing is made to be higher than a top surface of said transparent member, and further wherein a line between said pair of positioning holes and a line between said pair of attaching holes intersect with each other substantially at a center of said package and further wherein the line between the positioning holes is skewed with respect to each of ~~the two~~ four primary side walls of the housing and the line between the attaching holes is skewed with respect to each of ~~the~~ four primary side walls such that the line between the positioning holes and the line between the attaching holes are each neither parallel nor perpendicular to ~~either~~ any of the primary side walls, and neither line is located at a center line of the device which is perpendicular to the primary side walls.

6. (Original) The semiconductor device housing according to claim 5, wherein said semiconductor element is a solid-state imaging element.